What is claimed is:

~~CLAIMS~~

1. A charge sampling (CS) circuit (1), **characterised** by a control signal generator (4) for controlling an analog input signal to the charge sampling circuit (1) to be integrated by an intergrator (3) during a sampling phase responsive to a sampling signal from the control signal generator (4), wherein the current of the analog input signal is integrated to an integrated charge for producing a proportional voltage or current sample at a signal output at the end of the sampling phase.

2. A charge sampling (CS) circuit (1) according to claim 1, **characterised** by a sampling switch (2) having a signal input for analog input signals, a signal output connected to a signal input of said integrator (3), and a control input connected to a sampling signal output of said control signal generator (4) for controlling the switch to be on only when said sampling signal from the generator (4) is in a sampling phase.

3. A charge sampling (CS) circuit (1) according to claim 1 ~~or 2~~, **characterised** in that the control signal generator (4) is adapted to control the integrator (3) to hold the sample until a resetting signal from the generator (4) is applied to a control input of the integrator (3).

4. A charge sampling (CS) circuit (1) according to ~~any of the~~ claims 1~~-3~~, **characterised** in that

if said sampling phase is from time t_1 to time t_2, said sample represents the instant value of said analog signal at time $t_s=(t_1,+t_2)/2$ and differs from said instant value with a coefficient consisting of a constant part and a frequency dependent part $(\sin(2\pi f_i\Delta t))/(2\pi f_i\Delta t)$, where f_i is the frequency of the ith component of said analog signal

and $\Delta t=(t_2-t_1)/2$, i.e half of the width of said sampling phase.

5. A differential charge sampling (CS) circuit, **characterised** by a first and second CS circuit according to ~~any of the~~ claims 1-4 ~~having~~, wherein all control signal generators of said CS circuits are replaced by a common control signal generator (4), the signal input of said first CS circuit is a first analog input of said differential CS circuit, the signal input of said second CS circuit is a second input of said differential CS circuit for a differential analog signal, the signal output of said first CS circuit and the signal output of said second CS circuit are the first signal output and the second signal output of said differential CS circuit.

6. A differential charge sampling (CS) circuit according to claim 5, **characterised** in that the integrator (3) of said first CS circuit and the integrator (3) of said second CS circuit forming a single differential integrator with two inputs for integrating the differential current of said analog signal and producing differential samples at said first signal output and a second signal output.

7. A band-pass charge sampling (BPCS) circuit (5), **characterised** by a control signal generator (7) for controlling a first and second end of a differential analog signal to be weighted by a weighting-and-sampling (W&S) element (6) during a W&S phase responsive to a W&S signal from said control signal generator (7), wherein the current of said analog signal passes through said W&S element (6) only when said W&S signal is in a W&S phase, and said control signal generator (7) is adapted for controlling the output signal of said W&S element (6) to be integrated by an intergrator (3) during said W&S phase, wherein the

current of the output signal of said W&S element (6) is integrated to an integrated charge for producing a proportional voltage or current sample at a signal output at the end of said W&S phase.

8. A band-pass charge sampling (BPCS) circuit (5) according to claim 7, **characterised** by a first switch (2A) having a signal input for receiving a first end of said differential analog signal, a signal output connected to a signal input of said Weighting-and- sampling (W&S) element (6), and a control input connected to a clock output of said control signal generator (7) for controlling the switch (2A) to be on only when a clock signal is received, a second switch (2B) having a signal input for receiving a second end of said differential analog signal, a signal output connected to said signal input of said Weighting-and-sampling (W&S) element (6), and a control input, connected to an inverse clock output output of said control signal generator (7) for controlling the switch (2B) to be on only when a clock signal is received, said weighting-and-sampling (W&S) element (7) having a control input connected to a W&S signal output of said control signal generator, wherein the current of said analog signal passes through said W&S element (6) only when said W&S signal is in a W&S phase containing n cycles of said clocks, and the current of said analog signal is controlled by said W&S signal in constant, linear, Gauss or other weighting functions, and an integrator with a signal input connected to the output of said W&S element (6), a control input connected to a resetting signal output of said control signal generator (7).

9. A band-pass charge sampling (BPCS) circuit (5) according to claim 7 ~~or 8~~, **characterised** in that the control signal generator (7) is adapted to control the inte-

grator to hold the sample until the resetting phase of said resetting signal begins.

10. A band-pass charge sampling (BPCS) circuit (5) according to ~~any of the~~ claims 7~~-9~~, **characterised** in that said samples represent the base-band content of said analog signal, and the output frequency is $f_{out}=|f_{in}-(2p-1)f_c|$ for $2(p-1)f_c \leq f_{in} \leq pf_c$, where f_{in} is one of the frequency components of said analog signal, f_c the frequency of said clock and p an integer of ≥1 respectively, and the phase of said output frequency depends on the phase of said f_{in} and the phase of said f_c and p=1 defines the major frequency response range, and the same shape of frequency response is repeated for p>1 but the amplitudes are reduced, and for a given p, the same output frequency is obtained for frequencies f_{in1} ($<(2p-1)f_c$) and f_{in2} ($>(2p-1)f_c$) when $(2p-1)f_c-f_{in1}=f_{in2}-(2p-1)f_c$ but with different phases, and the bandwidth and the shape of said frequency response depend on said n (the lager n, the narrower bandwidth) and said weighting function (constant, linear, Gauss or other functions), and said BPCS circuit is simultaneously a filter, a mixer and a sampler.

11. A differential band-pass charge sampling (BPCS) circuit (8), **characterised** by a first and second BPCS circuit according to ~~any of the~~ claims 7~~-10~~, wherein all control signal generators of said BPCS circuits are replaced by a common control signal generator (7), the first signal input and the second signal input of said first BPCS circuit are connected with the second input and the first input of said first BPCS circuit respectively, and the first signal input, the second signal input, the signal output of said first BPCS circuit and the signal output of said second BPCS circuit are the first signal input, the second signal input, the first signal output and the second

signal output of said differential band-pass charge sampling (BPCS) circuit.

12. A differential band-pass charge sampling (BPCS) circuit (8) according to claim 11, **characterised** in that the integrators (3A,3B) in said first BPCS circuit and said second BPCS circuit are merged into a single differential integrator (10) integrating the differential current of said analog signal and producing differential samples at said first signal output and said second signal output of said differential BPCS circuit.

13. A parallel CS circuit, comprising a number of CS circuits according to ~~any of the preceding~~ claims ~~1-4~~, **characterised** in that all first signal inputs are connected together as a first analog signal input of said parallel CS circuit, all control signal generators of said CS circuits are replaced by a common control signal generator, a multiplexer having said number signal inputs connected to the signal outputs of said CS circuits respectively, control inputs connected to multiplexing signal outputs of said common control signal generator, and a signal output, for multiplexing the outputs of said CS circuits to the output of said parallel CS circuit when the outputs of said CS circuits are in holding phases, wherein said parallel CS circuit increases the sampling rate and makes the time interval between two successive sampling points short, and the parallel CS circuit is in a single ended version.

14. A parallel CS circuit, comprising a number of differential CS circuits according to claim 5 ~~or 6~~, **characterised** in that all first inputs are connected together as the first signal input of said parallel CS circuit for receiving a first end of a differential analog signal, all

second inputs are connected together as the second signal input of said parallel CS circuit for receiving a second end of said differential analog signal, and all control signal generators of said CS circuits are replaced by a common control signal generator, a multiplexer having said number signal input pairs connected to the signal output pairs of said CS circuits respectively, control inputs connected to multiplexing signal outputs of said common control signal generator, and a signal output pair, for multiplexing the output pairs of said CS circuits to the output pair of said parallel CS circuit when the output pairs of said CS circuits are in holding phases, wherein said parallel CS circuit increases the sampling rate and makes the time interval between two successive sampling points short, and the parallel CS circuit is in a differential version.

15. A parallel CS circuit according to claim 13 ~~or 14~~, **characterised** in that said control signal generator has a clock input, said number of sampling signal outputs, said number of resetting signal outputs and said number of multiplexing signal outputs, for generating said number of sampling signals at the sampling signal outputs connected to the control inputs of the switches of said CS circuits respectively, and for generating said number of resetting signals at said resetting signal outputs connected to the control inputs of the integrators of the CS circuits respectively, and said number of multiplexing signals are generated at the multiplexing signal outputs, and said resetting signals, said sampling signals and said multiplexing signals are evenly timeinterleaved.

16. A parallel BPCS circuit (11) comprising a number of BPCS circuits according to claim 7~~-10~~, **characterised** in that all first signal inputs are connected together as the

first signal input of said parallel BPCS circuit for receiving a first end of a differential analog signal, all second signal inputs are connected together as the second signal input of said parallel BPCS circuit for receiving a second end of a differential analog signal, and all the first switches are separate or merged, and all the second switches are separate or merged, and all control signal generators in said BPCS circuits are replaced by a common control signal generator (13), and a multiplexer (11) having said number of signal inputs connected to the signal outputs of said BPCS circuits, control inputs connected to multiplexing signal outputs of said common control signal generator, and a signal output, for multiplexing the outputs of said BPCS circuits to the signal output when the signal outputs of said BPCS circuits are in holding phases, wherein the signal output is the signal output of said parallel BPCS circuit, and said parallel BPCS circuit increases the sampling rate and makes the time interval between two successive sampling points smaller, and the parallel BPCS circuit is in a single ended version.

17. A parallel BPCS circuit (11) comprising a number of BPCS circuits according to claim 11 ~~or 12~~, **characterised** in that all first signal inputs are connected together as the first signal input of said parallel BPCS circuit for receiving a first end of a differential analog signal, all second signal inputs are connected together as the second signal input of said parallel BPCS circuit for receiving a second end of a differential analog signal, all the first switches in said first BPCS circuits are separate or merged, all the second switches in said first BPCS circuits are separate or merged, all the first switches in said second BPCS circuits are separate or merged, all the second switches in said second BPCS circuits are separate or merged, all control signal generators of said BPCS circuits

are replaced by a common control signal generator, and a multiplexer with said number of signal input pairs connected to the signal output pairs of said BPCS circuits, control inputs connected to multiplexing signal outputs of said common control signal generator, and an output pair, for multiplexing the output pairs of said BPCS circuits to the signal output pair when the signal output pairs of said BPCS circuits are in holding phases, wherein the signal output pair is the signal output pair of said parallel BPCS circuit, and said parallel BPCS circuit increases the sampling rate and makes the time interval between two successive sampling points smaller, wherein the parallel BPCS circuit is in a differential version.

18. A parallel BPCS circuit comprising a number of BPCS circuits according to claim 16 ~~or 17~~, characterised by a control signal generator with a clock input, a clock output, an inverse clock output, said number of W&S signal outputs, said number of resetting signal outputs and said number of multiplexing signal outputs, wherein the clock input is the clock input of said parallel BPCS circuit for use in generating a clock signal at the clock output of said common signal control generator connected to the control inputs of all first switches of said BPCS circuits, and an inverse clock at the inverse clock output connected to the control inputs of all second switches of said BPCS circuits, said number of W&S signal outputs are connected to the control inputs of all W&S elements (9A-9X) of said BPCS circuits, said number of resetting signal outputs are connected to the control inputs of all integrators (10A-10X) of said BPCS circuits, and said number of multiplexing signals, resetting signals, sampling signals, and multiplexing signals are evenly timeinterleaved.

19. A CS circuit according to any of the claims ~~1-4, or 13~~, **characterised** by an analog frequency compensating circuit having a signal input for receiving an analog signal, and a signal output, with a frequency response proportional to $(2\pi f_i \Delta t)/(\sin(2\pi f_i \Delta t))$, wherein the signal output is connected to the signal input of said CS.

20. A CS circuit according to any of the claims 5, ~~6, or 14~~, **characterised** by an analog frequency compensating circuit having a signal input pair for receiving an analog signal, and a signal output pair, with a frequency response proportional to $(2\pi f_i \Delta t)/(\sin(2\pi f_i \Delta t))$, wherein the signal output pair is connected to the first signal input and the second signal input of said CS circuit.

21. A CS circuit according to any of the claims ~~1-4, or 13~~, **characterised** by a digital frequency compensating circuit with a frequency response proportional to $(2\pi f_i \Delta t)/(\sin(2\pi f_i \Delta t))$ connected after an A/D converter converting the signal output of said CS circuits to a digital signal.

22. A CS circuit according to any of the claims ~~5-6, or 14~~, **characterised** by a digital frequency compensating circuit with a frequency response proportional to $(2\pi f_i \Delta t)/(\sin(2\pi f_i \Delta t))$ connected after an A/D converter converting the signal output pair of said CS circuits to a digital signal.

23. A two-step BPCS circuit comprising a first and second BPCS circuit (39,42) according to ~~any of the preceding~~ claims ~~6-12 or 16-18~~, **characterised** by

a first signal input and a second signal input for receiving a first and second end of a differential analog

signal, respectively, in said first BPCS circuit (39) for producing signal samples at the signal output or output pair of said first BPCS circuit with a first sample rate;

a chopping circuit (40) for chopping the signal from the first BPCS circuit (39) symmetrically in time at its signal output or output pair with the frequency of a clock signal equal to said first sample rate,

a differential-out amplifier (41) for amplifying the signal from the chopping circuit differentially at its signal output pair; and

the first signal input and the second signal input of said second BPCS are connected to the signal output pair of said amplifier (41) for producing signal samples at the signal output or output pair with a second sample rate.

24. A two-step BPCS circuit comprising according to claim 23, **characterised** by a clock signal generator (43) having a clock input for receiving a first clock signal used by the first BPCS circuit (39), and generating a second clock signal simultaneously fed to a clock input of said chopping circuit and a clock input of said second BPCS circuit.

25. Arrangements of building blocks in any type of said BPCS circuits according to claims ~~1-24~~ 24, **characterised** by

an n-MOS arrangement of said switch, comprising: an n-MOS transistor with the drain as the signal input, with the gate as the control input and with the source as the signal output; and

a CMOS arrangement of said switch, comprising: an n-MOS transistor and a p-MOS transistor with their drains connected to each other as the signal input, with their sources connected to each other as the signal output, and with the gate of said n-MOS transistor as the control

input; an inverter with the input connected to the gate of said n-MOS transistor and with the output connected to the gate of said p-MOS transistor;

an arrangement of said W&S element, comprising: an n-MOS transistor with the drain as the signal input, with the gate as the control input, and with the source as the signal output;

a passive arrangement of said integrator, comprising: a capacitor with the first end as the signal input, and with the second end grounded; an optional resistor inserted between said signal input and the first end of said capacitor when necessary; an n-MOS transistor with the drain and the source connected to the first end and second end of said capacitor respectively, and with the gate as the control input;

a passive arrangement of said differential integrator comprising: a first passive arrangement of said integrator with the signal input and the signal output as the first signal input and the first signal output of said differential integrator respectively; and a second passive arrangement of said integrator with the signal input and the signal output as the second signal input and the second signal output of said differential integrator respectively;

an active arrangement of said integrator comprising: a differential-in-single-out amplifier with the positive input grounded, with the negative input as the signal input of said integrator, and with the output as the signal output of said integrator; a capacitor with the first end connected to the negative input of said differential-in-single-out amplifier; an inverter with the input as the control input of said integrator; a first n-MOS arrangement or CMOS arrangement of said switch with the signal input connected to the negative input of said differential-in-single-out amplifier, with the control input connected to the control input of said integrator,

and with the signal output connected to the output of said differential-in-single-out amplifier; a second n-MOS arrangement or CMOS arrangement of said switch with the signal input connected to the second end of said capacitor, with the control input connected to the control input of said integrator, and with the signal output grounded; a third n-MOS arrangement or CMOS arrangement of said switch with the signal input connected to the second end of said capacitor, with the control input connected to the output of said inverter and with the signal output connected to the output of said differential-insingle-out amplifier; and an optional resistor inserted between the signal input of said integrator and the negative input of said differential-in-single-out amplifier when necessary;

an active arrangement of said differential integrator, comprising: a differential-in-differential-out amplifier with the negative input, the positive input, the positive output and the negative output as the first signal input, the second signal input, the first signal output and the second signal output of said differential integrator; a first capacitor with the first end connected to the negative input of said differential-indifferential-out amplifier; a second capacitor with the first end connected to the positive input of said differential-in-differential-out amplifier; an inverter with the input as the control input of said differential integrator; a first n-MOS arrangement or CMOS arrangement of said switch with the signal input connected to the negative input of said differential-in-differential-out amplifier, with the control input connected to the control input of said differential integrator and with the signal output connected to the positive output of said differential-in-differential-out amplifier; a second n-MOS arrangement or CMOS arrangement of said switch with the signal input connected to the second end of said first capacitor,

with the control input connected to the control input of said differential integrator and with the signal output grounded; a third n-MOS arrangement or CMOS arrangement of said switch with the signal input connected to the second end of said first capacitor, with the control input connected to the output of said inverter and with the signal output connected to the positive output of said differential-in-differential-out amplifier; a fourth n-MOS arrangement or CMOS arrangement of said switch with the signal input connected to the positive input of said differential-in-differential-out amplifier, with the control input connected to the control input of said differential integrator and with the signal output connected to the negative output of said differential-in-differential-out amplifier; a fifth n-MOS arrangement or CMOS arrangement of said switch with the signal input connected to the second end of said second capacitor, with the control input connected to the control input of said differential integrator and with the signal output grounded; a sixth n-MOS arrangement or CMOS arrangement of said switch with the signal input connected to the second end of said second capacitor, with the control input connected to the output of said inverter and with the signal output connected to the negative output of said differential-in-differential-out amplifier; a first optional resistor inserted between the first signal input of said differential integrator and the negative input of said differential-in-differential-out amplifier when necessary; and a second optional resistor inserted between the second signal input of said differential integrator and the positive input of said differential-in-differential-out amplifier when necessary.

26. A front-end sampling radio receiver apparatus comprising a first and second BPCS circuit according to claims ~~7,12,16-18,23,24~~, **characterised** by comprising:

a low pass filter (45) with a bandwidth up to twice the clock frequency for receiving and filtering a radio signal;

a low noise amplifier (46) for producing a differentially amplified radio signal from the filtered signal;

a local oscillator (49) for producing an I-clock signal at its signal output;

a $\pi/2$ phase shifter (48) with a signal input connected to the local oscillator (49) for producing a Q-clock signal at its signal output with the same amplitude and $\pi/2$ phase shift with respect to said I-clock signal;

two ends of the signal output pair of said low noise amplifier (46) are respectively connected both to the first BPCS circuit (47A) and the second BPCS circuit (47B) respectively, said I-clock signal output is connected to the clock input of said first BPCS circuit (47A), and said Q-clock signal output is connected to the clock input of said second BPCS circuit (47B), for producing base-band I-samples of said radio signal at the signal output or output pair of said first BPCS circuit (47A), base-band Q - samples of said radio signal at the signal output or output pair of said second BPCS circuit (47B).

27. A front-end sampling radio receiver apparatus according to claim 26, **characterised** in that

said local oscillator (49), said phase shifter (48) and the clock generators of said first and second BPCS circuits (47A,47B) are combined for producing differential I-clock signals and Q-clock signals more efficiently and accurately;

said base-band I-sample and Q-samples are converted either by two separate analog-to-digital converters or by a

single analog-to-digital converter with multiplexing to digital signals;

said digital signals are processed by a digital signal processing (DSP) unit; and

said front-end sampling radio receiver apparatus is a superior radio receiver apparatus having a greatly simplified analog part and wherein the capability of DSP is highly utilized.

28. A method of charge sampling, **characterised** by the steps of:

integrating an analog input signal during a sampling phase, wherein the current of the analog input signal is integrated to an integrated charge, and

producing a proportional voltage or current sample of said integrated charge at the end of said sampling phase.

29. A method according to claim 28, **characterised** in that, if said sampling phase is from time t_1 to time t_2, said sample represents the instant value of said analog signal at time $t_s=(t_1+t_2)/2$ and differs from said instant value with a coefficient consisting of a constant part and a frequency dependent part $(\sin(2\pi f_i \Delta t))/(2\pi f_i \Delta t)$, where f_i is the frequency of the ith component of said analog signal and $\Delta t=(t_2-t_1)/2$, i.e half of the width of said sampling phase.

30. A method according to claim 28 ~~or 29~~, **characterised** in that said analog input signal is a differential analog signal, and said proportional voltage or current sample of said integrated charge is a differential signal.

31. A method of charge sampling, **characterised** by the steps of: weighting a first and second end of a differential analog signal during a W&S phase, integrating the

weighted signal during said W&S phase, wherein the current of the weighted signal is integrated to an integrated charge; and

producing a proportional voltage or current sample at the end of said W&S phase.

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